REMARKS

In the above referenced Office Action, the Examiner rejected claims 1-34 under 35 USC § 103(a) as being unpatentable over Brown et al. (U.S. Patent No. 6,792,578) in view of Lee et al.(U.S. Patent No. 6,502,229) or in view of Wang et al.(U.S. Patent No. 6,594,809). These rejections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-34.

As mentioned above, claims 1-34 of the present application were rejected based on the combination of Brown with Lee or based on the combination of Brown with Wang. Applicant respectfully submits that that the combination of Brown with either Lee or Wang is improper. Lee and Wang each present circuit design methodologies based on detected antenna rule violations. By contrast, Brown presents an integrated circuit design that avoids the reliance on the detection of antenna rule violations and, instead, presents a brute force multilayer design that connects trace segments with vias to avoid the build-up of harmful static charge over a broader number of circuit elements, but at the expense of greater design complexity. Brown justifies this approach by stating:

> "If a violation of the antenna rule is determined to occur at I/O port 12, one of the methods of the prior art discussed above can be used to eliminate the problem. Unfortunately, as mentioned above, those methods are not always successful at detecting antenna rule violations and, even if detected, the repair of an antenna rule violation can be difficult due to the limited area that is available to perform the fix. The present invention improves the design of the hard macro to eliminate antenna rule violations and, thus, the need to check for them." (Col. 3, lines 59 – 67).

By rejecting the rule violations approach, Brown teaches away from Applicant's invention as embodied in claims 1-34 and likewise teaches away from both Lee and Wang. For this reason, the combinations of Brown with Lee and Brown with Wang are improper. Applicant thus believes that claims 1-34 are patentably distinct from the prior art.

Claim 7 presents a method for correcting antenna violations in high-density integrated circuits in accordance with an embodiment of the present invention. This

embodiment includes the steps of determining a cell of the integrated circuit based on the error coordinates and a design exchange format file, determining error position within the cell based on the error coordinates, and determining an affected input of the cell based on the error position and a library exchange file. Examiner cites Brown as disclosing these steps. While Applicant believes that Brown is not a proper reference as discussed above, Applicant also respectfully submits that Brown does not disclose, suggest or teach the specific steps set forth above. For instance, the step of determining an affected input of the cell based on error position and a library exchange file is not disclosed by Brown. Brown presents no disclosure of library exchange files. This provides a separate and independent reason that claim 7 and claims 8-13 that depend therefrom are patentably distinct from the prior art.

Claim 11 further refines claim 7 by the following recital:

> interpreting the library exchange file to determine inputs and outputs of the cell;
> determining location of the inputs within the cell; and
> identifying one of the inputs as the affected input based on the location of the one of the inputs being proximal to the error position.

None of these additional steps are disclosed, suggested or taught by Brown. Brown's general disclosure of netlists is insufficient to teach or suggest these specific steps. This provides an additional basis for Claim 11 to be patentably distinct from the prior art.

Claims 20 and 24 include elements similar to the elements discussed above in conjunction with Claims 7 and 11. In particular, claim 20 is directed to an integrated circuit in accordance with an embodiment of the present invention that determines a cell of the plurality of cells based on the error coordinates and a design exchange format file, determines error position within the cell based on the error coordinates, and determines an affected input of the cell based on the error position and a library exchange file. Claim 24 further interprets the library exchange file to determine inputs and outputs of the cell, determines the location of the inputs within the cell, and identifies one of the inputs as the affected input based on the location of the one of the inputs being proximal to the error position. As discussed above, Brown does not disclose, suggest or teach these particular features. This provides a separate basis for claim 20, claim 24, and claims 21-23 and 25-26 that depend from claim 20, to be

patentably distinct from the prior art.

For the foregoing reasons, the applicant believes that claims 1-34 are in condition for allowance and respectfully request that they be passed to allowance.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicant
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 6, 2005.

Pat Slaback
Name

Signature